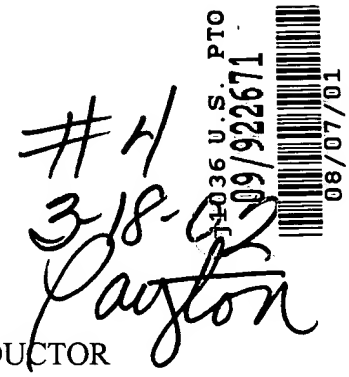
Docket No.: 60188-084 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re Application of	:	
Shigeki FURUYA, et al.	:	
Serial No.:	:	Group Art Unit:
Filed: August 7, 2001	:	Examiner:

For: CMOS BASIC CELL AND METHOD FOR FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT USING THE SAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, DC 20231

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The relevance of each non-English language reference, if any, is discussed in the present specification.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

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